REMARKS

Applicants have amended the claims by canceling all previous claims and adding a new claim set in an effort to restrict the claims to subject matter indicated allowable in the outstanding Final Rejection. However, the present independent claims 29 and 35 do not restrict the substrate to glass as was the case in claims 19 and 25 indicted to be allowable in the outstanding Final Rejection. Canceled allowable claims 19 and 25 have been replace with new claims 29 and 35 which are believed to be allowable as are new dependent claims 30-34 and 36-39 which parallel the canceled dependent claims.

The rejection of claims 18 and 23 has been carefully considered but is most respectfully traversed in view of the amendment to the claims and the cancellation of these claims from the application without prejudice or disclaimer. It is believed that the amendment to the claims obviates the rejection over the prior art and under 35 USC 112 as set forth in the final rejection and restricts the claims to the allowable subject matter. Accordingly, it is most respectfully requested that the rejection under 35 USC 112 and the prior art rejections be withdrawn.

Figures 1 and 2 are not relevant to the presently claimed subject matter and may be deleted by Examiner's amendment should the Examiner believe this appropriate. Only drawing Figure 3 is germane as the new claim set relates thereto. All of the previously presented claims have been canceled from the application without prejudice or disclaimer and replaced with new claims 29-39 as fully supported by Applicants' specification as originally filed and as would be appreciated by one of ordinary skill in the art to which the invention pertains.

The informalities of claims 18 and 23 as noted in the Final Rejection have been obviated by the cancellation of these claims. Accordingly, it is most respectfully requested that the rejection of these claims under 35 USC 112 be withdrawn.

Applicants most respectfully submit that all the claims now present in the application are in full compliance with 35 U.S.C. 112 and are clearly patentable over the references of record.

The rejection of claims 17, 18, 21, 23, 24 and 27 under 35 U.S.C. 103(a) as being unpatentable over Zhang et al., in view of Jiroku et al. and claims 20, 22, 26 and 28 as being unpatentable over Zhang in view of Jiroku as applied to claims 17 and 23 above, and further in view of Yamazaki et al. have been carefully considered but is most respectfully traversed in view of the amendment to the claims to restrict the claims to allowable subject matter.

Claim 29 relates to allowable claim 19 written in independent form to include the limitation of the intervening claims which are believed to distinguish over the prior art as noted in the outstanding Final Rejection. Claim 35, which is a new method claim similar to but not identical to claim 29, and is also believed to contain the subject matter indicated to be allowable in the outstanding Final Rejection. Please note that these claims are not the same as the allowable claims but are believed to contain the combination of subject matter which the Examiner indicated to be allowable.

Applicants will now discuss the differences between Applicants' invention and the prior art as follows:

Difference between the heating plate crystallization technique and Zhang

Different characteristics for selected metal

The selection metal according to the present invention is required to provide the characteristics of better infrared absorbability and higher thermal stability (such as MoW, Cr, etc.), but is not required to be of the catalysis characteristic (with a-Si layer). However, in the Zhang patent, the selected metal is required of the substance with catalysis characteristic (with a-Si layer) (such as Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Sc, Ti, V, Cr, Mn, Cu, Zn, Au, Ag, etc.).

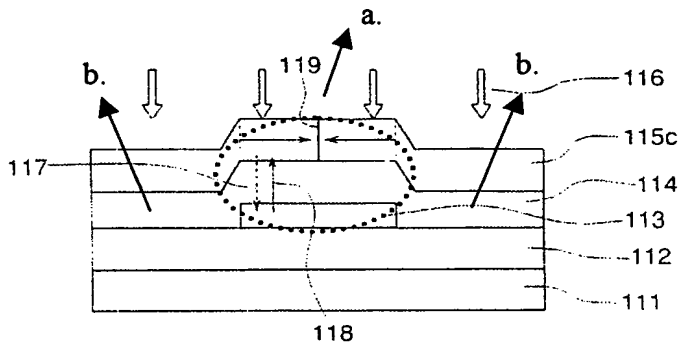
Different crystallization manner and mechanism

The present invention employs the metal in heating plate area to absorb the infrared rays emitted by the pulsed rapid thermal annealing process (PRTP), which will induce the rapid vibration of phonon in the heating plate area, and the energy obtained from the rapid vibration can be indirectly transferred to the a-Si layer by the thermal conduction, so the a-Si layer will form the poly-Si. However, in the Zhang patent, it employs the metal with catalysis characteristic (with a-Si layer) to infiltrate into the a-Si film, and forms the metal silicide with a-Si, which employs the feature of differences between lattice constants of the two, about 0.4% between metal silicide (such as $NiSi_2$: 5.406A) and crystallized silicon molecule (5.43A), so as to employ the metal silicide as the crystal seed; employing the following thermal process to form the crystal of a-Si layer under the metal as the poly-Si.

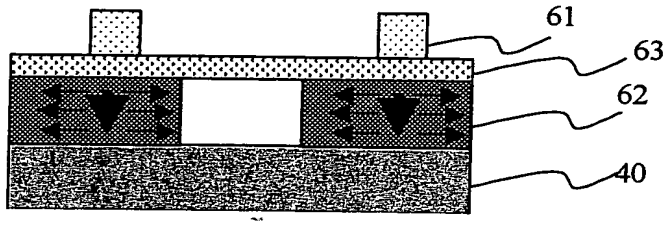
Differences between heating plate crystallization technique and Jiroku

Different crystallization manner and mechanism

The Jiroku patent first employs the XeCl laser to irradiate on the semiconductor layer to form the Poly-Si (115c); employing YAG2 ω (116) solid laser to irradiate through the semiconductor layer (115c) onto the semiconductor layer (113) to cause partial reflection, and the reflection light (118) will be reflected onto the semiconductor layer (115c) to cause the temperature of the upper area of semiconductor layer (113) relatively higher than other areas. With the temperature difference between a- and b-areas (temperature in a-area is higher than b-area), the direction of crystallization will become crystallizing from both left and right sides toward the center, as shown in the following figure.

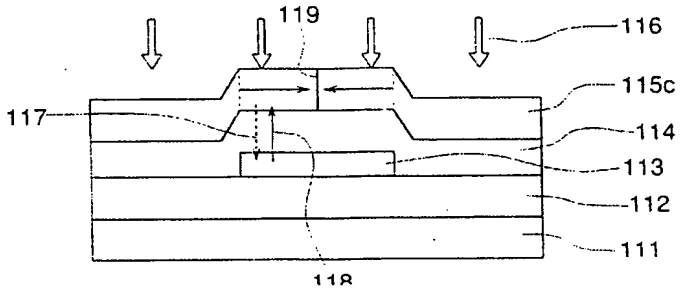


However, the present invention employs the heating plate area (61) to absorb the infrared rays emitted by the pulsed rapid thermal annealing process (PRTP), which will induce the rapid vibration of phonon in the heating plate area, and the energy obtained form the rapid vibration can be indirectly transferred to the a-Si layer by the thermal conduction, so the a-Si layer will form the poly-Si (62).

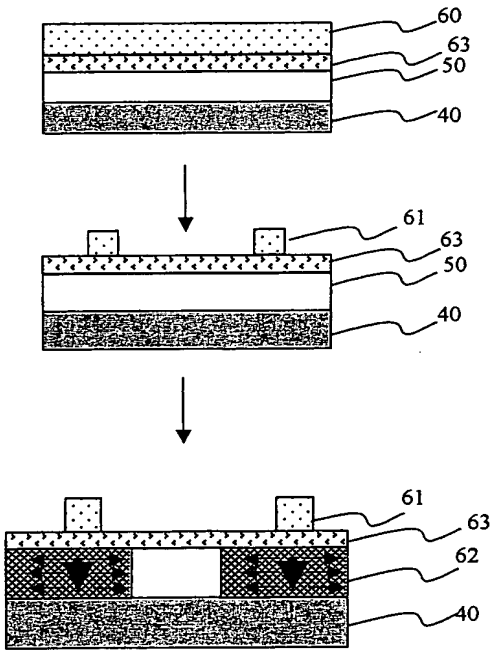


Different crystallization structure

The Jiroku patent must first deposit a semiconductor layer (113) on a substrate and employs the partial reflection of YAG2 ω (116) solid laser by the semiconductor layer (113) to cause the temperature of the upper area of semiconductor layer (113) relatively higher than other area. With the temperature difference between a- and b-areas (temperature in a-area is higher than b-area), the direction of crystallization will become crystallizing from both left and right sides toward the center and then conducting the fabrication of TFT device.



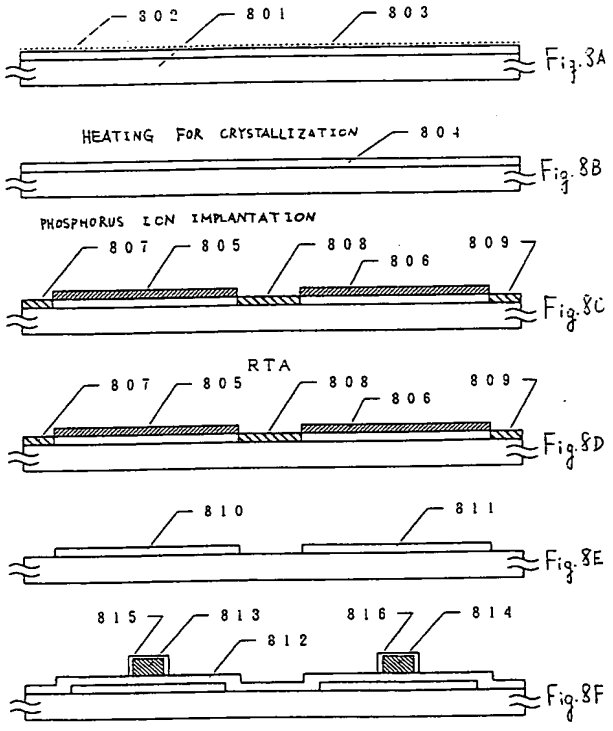
However, the present invention must deposit a metal layer (60) (such as MoW, Cr, etc.) with better infrared absorbability and highly thermal stability; employing photolithography and etching processes to form the metal layer in an island distribution, also called as the heating plate area (HP) (61), and employing the heating plate area (61) to absorb the infrared rays emitted by the pulsed rapid thermal annealing process (PRTP) to form the a-Si layer (50) as a Poly-Si layer (62). Then, it must employ etching process to remove the heating plate area (61) in an island distribution and the oxide layer (63) before conducting the fabrication of TFT device.



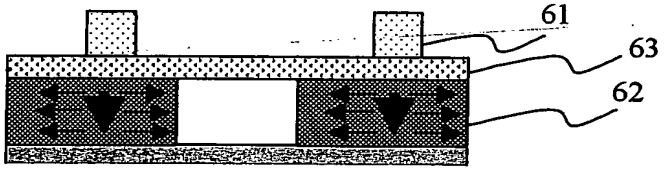
Difference between heating plate crystallization technique and Yamazaki

Different crystallization manner and mechanism

The Yamazaki patent first deposits a semiconductor layer (802) on a substrate; then, doping the substance with the catalysis characteristic (with a-Si layer) (such as Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag) on the semiconductor layer (802) to form the 803. Yamazaki has the metal with catalysis characteristics (with a-Si layer) infiltrated into the a-Si film to form the metal silicide with the a-Si. With the feature of differences between lattice constants of the two, about 0.4% between metal silicide (ishc as $NiSi_2$: 5.406A) and crystallized silicon molecule (5.430A), Yamazaki employs the metal silicide as the crystal seed; employing the following thermal process to form the crystal of a-Si layer under the metal as the poly-Si (804).

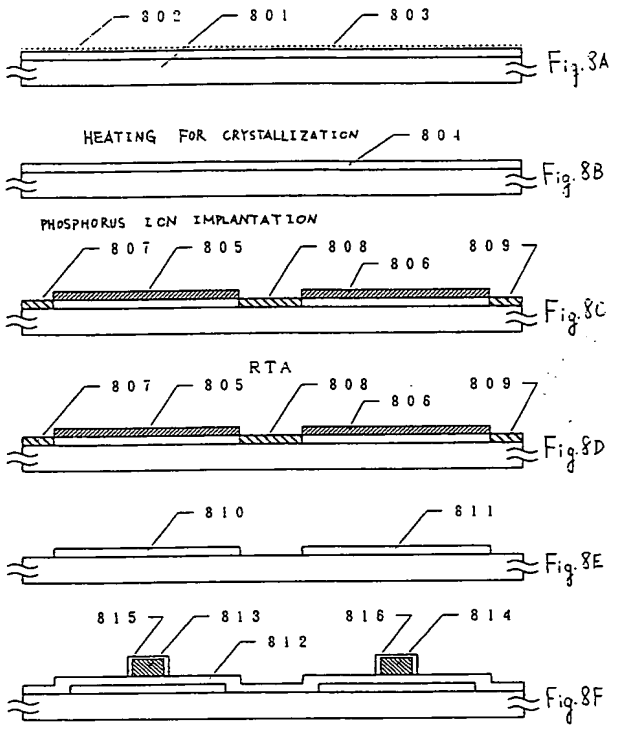


However, the present invention employs the heating plate area (61) to absorb the infrared rays emitted by the pulsed rapid thermal annealing process (PRTP), which will induce the rapid vibration of phonon in the heating plate area, and the energy obtained from the rapid vibration can be indirectly transferred to the a-Si layer by the thermal conduction, so the a-Si layer will form the poly-Si.

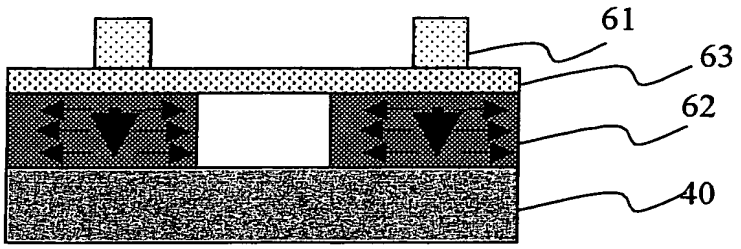


Different roles played by RTA and PRTP

The Yamazaki patent is to deposit the metal (W, Cr, Mo. Ti) on the Poly-Si (804); employing photolithography and etching processes to define the patterns 805, 806; using 805, 806 as a hard mask to conduct the ion implantation of phosphor ions (P+) to form 807, 808, 809; employing the RTA to render thermal energy to induce the substance with catalysis characteristic (with a-Si layer) (such as Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag) to move left and right, and finally being captured in 807, 880, 809 areas; using etching process to remove 805, 806, 807, 808 and 809; and finally conducting the fabrication of TFT device.



However, the present invention employs the heating plate area (61) in an island distribution to absorb the infrared rays emitted by the pulsed rapid thermal annealing process (PRTP), which will induce the rapid vibration of phonon in the heating plate area, and the energy obtained from the rapid vibration can be indirectly transferred to the a-Si layer by the thermal conduction, so the a-Si layer will form the Poly-Si; using etching process to remove the heating plate area (61) in an island distribution and the oxide layer (63); and then conducting the fabrication of TFT device.



Furthermore, Applicants wish to direct the Examiner attention to the basic requirements of a prima facie case of obviousness as set forth in the MPEP 2143. This section states that to establish a prima facie case of obviousness, three basic criteria first must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. For the above reasons, a prima facie case of obviousness has not been established and the rejections should be withdrawn. Accordingly, it is most respectfully requested that this rejection be withdrawn in view of the amendments to the claims and the above discussion.

Please also see Enclosures 1 and 2 attached for figures of the TFT process and the present invention.

In view of the above comments and further amendments to the claims, favorable reconsideration and allowance of all of the claims now present in the application are most respectfully requested.

Respectfully submitted,
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A02.wpd
July 8, 2005

Enclosure 1

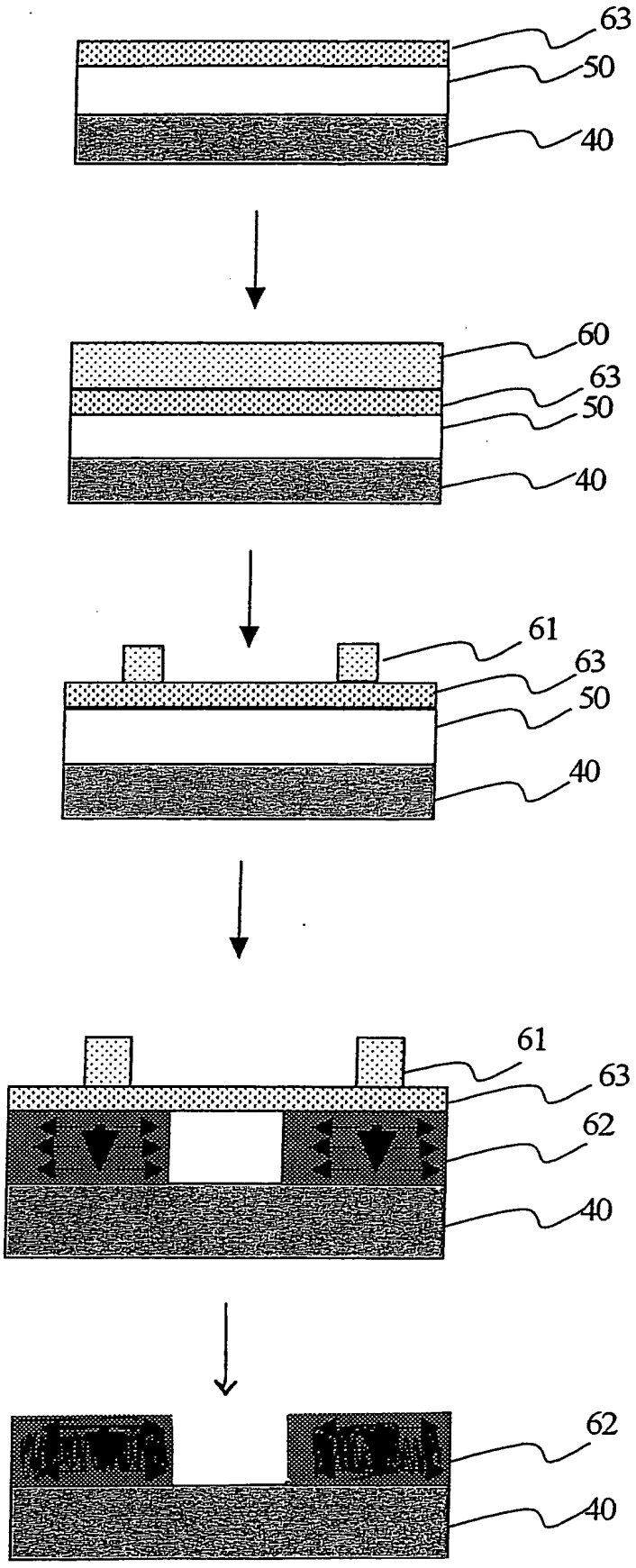
Information Sheet

1. Complement Abstract for Heating Plate Crystallization

The present invention provides a heating plate crystallization fabrication method, which is suitable for crystallization process of poly-silicon thin film transistor as a Heating Plate Crystallization (HPC) fabrication method. The present method is a fabrication method for Heating Plate Crystallization (HPC) using pulsed rapid thermal annealing process, which includes the following steps: employing physical vapor deposition or chemical vapor deposition to continuously deposit a-Si(50)/ oxide (63) on a substrate (40); employing physical vapor deposition or chemical vapor deposition to deposit a metal layer (60) (such as MoW, Cr, etc.) providing a better absorbability to infrared and highly thermal stability; employing yellow light and etching process to form the metal layer in an island distribution, also called as heating plate (HP) area (61). The reason for forming the metal layer in an island distribution is that when the processing temperature for pulsed rapid thermal annealing process (PRTP) is larger than 700 Celsius degree, because the heating plate area is in an island distribution, the glass substrate (deformation temperature about 660 Celsius degree) can only endure thermal energy in local areas and will not occur the glass deformation due to too high a processing temperature.

Employing pulsed rapid thermal annealing process (PRTP) for absorbing infrared by the heating plate area in island distribution, it will induce the rapid vibration of phonon in the heating plate area, and the energy obtained from the rapid vibration can be indirectly transferred to the a-Si layer through the thermal conduction, so the a-Si layer (50) can obtain sufficient energy of crystallization to form the poly-Si (62); using etching process to remove the heating plate area (61) and the sacrificing oxide layer (63) (the sacrificing oxide layer is existed between heating plate area and a-Si layer)

Enclosure 1



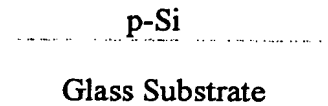
Enclosure 1

The Poly-Si islands can be defined by yellow light and etching process. However, within these islands, only a portion of areas need doping but the others are the channels of transistors; depositing the gate oxide; depositing the Gate Metal (called M1 hereinafter) on the oxide; defining M1 patterns through yellow light and etching processes; using M1 as the hard mask for N+ doping, and N+ doping defines the N-type TFTs source and drain areas; and achieving the self-aligned effect. After completion of N+ doping, a layer of TEOS oxide (interlayer) is deposited on the M1; digging the contact holes (defined by yellow light and etching processes)at the source and drain; filling the source/drain metal (called M2 hereinafter) into the contact holes; defining the pad for S/D and Metal 2 through yellow light and etching processes; depositing a layer of TEOS-oxide (Passivation) on the M2; using the pulsed rapid thermal annealing process (PRTP) to activate the heating plate, and absorbing infrared by the heating plate area M2; and indirectly transferring energy after heating to the N-type TFTs source and drain area in a thermal conduction manner to ion-activate the phosphor ions to form the S/D with low resistance. So far, the fabrication of Poly-Si TFT device is completed.

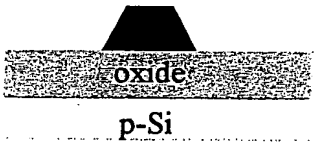
Enclosure 2

Reference diagram for TFT device fabrication

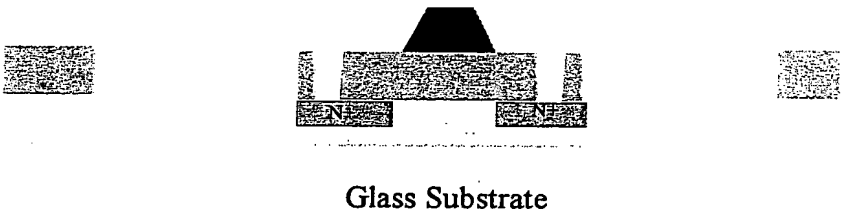
B. Poly-Si



C. Metal 1



D. Contact



E. Metal 2